

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1        1. (Currently Amended) A computer implemented method of  
2 multilevel dither screening comprising the steps of:  
3        defining a dither value for each pixel of a screening matrix;  
4        packing plural pixel values corresponding to plural pixels  
5 into equal sections of a first data word;  
6        packing plural corresponding dither values into said equal  
7 sections of a second data word;  
8        adding corresponding sections said first data word and said  
9 second data word in an arithmetic logic unit selectively spilttable  
10 into said equal sections thereby forming a sum data word;  
11        saturating any section of said sum data word generating ~~an~~ a  
12 carry output during ~~addition~~ said adding to a section of all 1's  
13 and passing other sections unchanged thereby forming a saturated  
14 sum data word; and  
15        truncating a predetermined number of least significant bits of  
16 each section of said saturated sum data word forming a dither  
17 screen data word.

1        2. (Original) The method of claim 1, wherein:  
2        said step of adding corresponding sections said first data  
3 word and said second data word further includes saving a carry out  
4 of each section in a multiple flags data word;  
5        said step of saturating any section of said sum data word  
6 generating an carry output during addition includes  
7        expanding said carry out of each section in said multiple  
8 flags data word to fill a corresponding section of a mask data  
9 word,

10 forming the logical OR of (1) a logical AND of a  
11 saturated data word having all 1's in every section and said  
12 mask data word, and (2) a logical AND of said sum data word  
13 and a logical inverse of said mask data word.

1 3. (Original) The method of claim 1, wherein:  
2 said step of truncating a predetermined number of least  
3 significant bits of each section of said saturated sum data word  
4 includes  
5 right shifting said saturated sum data word said  
6 predetermined number of bits,  
7 forming a mask data word having said predetermined number  
8 of 1's in least significant bits of each section and 0's in  
9 most significant bits of each section, and  
10 forming a logical AND of said shifted saturated sum data  
11 word and said mask data word.

1 4. (Currently Amended) The method of claim 1, wherein:  
2 said input pixel values are represented in a fixed point  
3 format of 8 bits including 4 integer bits and 4 fractional bits;  
4 said dither values are represented in a fixed point format of  
5 4 bits including zero integer bits and 4 fractional bits; and  
6 said predetermined number of least significant bits of said  
7 step of truncating is 4.

1 5. (Original) The method of claim 1, further comprising the  
2 step of:  
3 quantizing each section of said dither screen data word into a  
4 limited set of threshold ranges.

1        6. (Currently Amended) A printer comprising:  
2        a transceiver adapted for bidirectional communication with a  
3        communications channel;  
4        a memory;  
5        a print engine adapted for placing color dots on a printed  
6        page according to received image data and control signals; and  
7        a programmable data processor connected to said transceiver,  
8        said memory and said print engine, said programmable data processor  
9        including a selectively splittable arithmetic logic unit, said  
10        programmable data processor programmed to:  
11            receive print data corresponding to pages to be printed  
12            from the communications channel via said transceiver;  
13            convert said print data into image data and control  
14            signals for supply to said print engine for printing a  
15            corresponding page, said conversion including multilevel  
16            dither screening by  
17            defining a dither value for each pixel of a screening  
18            matrix,  
19            packing plural pixel values corresponding to plural  
20            pixels into equal sections of a first data word,  
21            packing plural corresponding dither values into said  
22            equal sections of a second data word,  
23            adding corresponding sections said first data word and  
24            said second data word in said arithmetic logic selectively  
25            spilt into said equal sections forming a sum data word,  
26            saturating any section of said sum data word generating  
27            ~~an~~ a carry output during ~~addition~~ said adding to a section of  
28            all 1's and passing other sections unchanged thereby forming a  
29            saturated sum data word; and  
30            truncating a predetermined number of least significant  
31            bits of each section of said saturated sum data word forming a  
32            dither screen data word.

1 7. (Original) The printer of claim 6, wherein:  
2 said programmable data processor further including  
3 a multiple flags register connected to said arithmetic  
4 logic unit receiving and storing a carry out from each of said  
5 sections of said arithmetic logic unit, and  
6 an expand circuit connected to said multiple flags  
7 register for expanding each bit of said multiple flags  
8 register to fill a corresponding section thereby forming a  
9 mask data word; and

10 wherein said programmable data processor is programmed to saturate  
11 any section of said sum data word generating an carry output during  
12 addition by

13 forming in said arithmetic logic unit the logical OR of  
14 (1) a logical AND of a saturated data word having all 1's in  
15 every section and said mask data word, and (2) a logical AND  
16 of said sum data word and a logical inverse of said mask data  
17 word.

1 8. (Currently Amended) The printer of claim 6, wherein:

2 said programmable data processor further including  
3 a selectable shifter,  
4 a mask generator having an input and an output filling  
5 each section with a number of least significant 1's equal to a  
6 number at said input and

7 wherein said programmable data processor is programmed ~~to~~ for  
8 truncating a predetermined number of least significant bits of each  
9 section of said saturated sum data word by

10 supplying said predetermined number to said shifter to  
11 right shift said saturated sum data word by said predetermined  
12 number of bits,

13           supplying said predetermined number to said input of said  
14 mask generator thereby forming a mask data word having said  
15 predetermined number of 1's in least significant bits of each  
16 section and 0's in most significant bits of each section, and  
17           forming in said arithmetic logic unit a logical AND of  
18 said shifted saturated sum data word and said mask data word.